Short–Open Calibration Technique for Field Theory-Based Parameter Extraction of Lumped Elements of Planar Integrated Circuits

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***Abstract*—A generalized short–open calibration (SOC) technique is developed toward complete field theory-based deembedding and lumped-element extraction of equivalent-circuit models for planar integrated circuits from admittance-type method of moments (MoM) simulations. With reference to the modal expansion modeling of a rectangular waveguide discontinuity, our investigation at first is to show the physical reason why there exist two aspects of numerical error in a deterministic MoM regarding a microstrip step discontinuity as the showcase in this study. In this SOC scheme, the identified two error sources are put together as a single error term or box for each feed line and then characterized by defining and evaluating two self-consistent calibration standards in the MoM, namely, *short* and *open elements*. As such, the core circuit model of the step discontinuity is effectively extracted by removing out two error terms. Subsequently, geometry- and frequency-dependent characteristics of the SOC technique are studied and discussed to demonstrate its effectiveness and accurateness as compared with the conventional transmission-line deembedding technique. After a series of validations by static analysis and measured results, the SOC scheme is used to model symmetrical and asymmetrical microstrip step discontinuities in terms of their equivalent dynamic circuit model over a wide frequency range.**

***Index Terms*—Equivalent-circuit model, lumped element, method of moments, microstrip step discontinuity, planar integrated circuits, short–open calibration.**

I. Introduction

FULL-WAVE method-of-moments (MoM) algorithms [1]–[4] have been extensively studied and developed for analysis and characterization of unbounded and shielded planar integrated circuits. User-friendly MoM-based simulation packages are commercially available,[1] which are widely popular for the design of planar integrated circuits of complex geometry on the basis of trial-and-error or direct electromagnetic (EM) field optimization procedure [5]. Considering the fact that such circuit layouts usually occupy electrically large areas, this field-based direct procedure becomes computationally intensive in practical design, requiring excessive computational resources, as well as multiple design circles. It is also difficult to gain physical insight into the operating mechanism of planar circuits in question because only external parameters are given from the MoM simulation over the whole circuit layout.

In fact, all electrically large planar circuits essentially consist of multiple lumped and/or electrically small elements such as bend, gap, step, T-junction, cross junction, coupled-line, etc. To undertake the efficient design procedure, the preferred approach is first to use the MoM for characterization of all those building elements of the whole planar circuit and then to deembed or extract their equivalent-circuit models at predesignated reference planes. Such models allow implementing various synthesis or optimization techniques of planar passive and active circuits in the design on the basis of a network-dominated topology. However, the use of MoM in the parameter extraction of the electrically small-circuit segments cannot be made straightforwardly and it is a challenging issue because the numerical errors in the MoM may override the inherent discontinuity effects of such elements to be considered. As a result, a special "noise-removal" technique should be developed to address this issue.

To our knowledge, several techniques were presented in [6]–[9] to deembed electrical parameters at certain internal locations along each feed line of a planar integrated circuit or discontinuity from the MoM-calculated parameters at certain corresponding source ports. Although examples were reported to validate the effectiveness of these techniques, no systematic work has thus far been carried out toward the establishment of a comprehensive scheme of the field-theory-based parameter extraction of equivalent-circuit models for electrically small or lumped planar elements, as described above.

Stemming from the calibration principle in microwave measurements [10], a generalized deembedding technique called the short–open calibration (SOC) technique [11] has recently been presented by the authors in a deterministic admittance-type MoM algorithm [4] to deembed and/or extract the equivalent dynamic circuit models of unbounded planar distributed and lumped circuits or discontinuities. As detailed in [11], two ideal calibration standards, i.e., *short* and *open elements*, are formulated and developed in the MoM framework for accurately characterizing the behavior of each feed-line section between a source port and its related reference plane. This

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[1]Commercial EM planar simulators such as Agilent Momentum, Ansoft Ensemble, Sonnet EM Suite, Jansen LINMIC+/N, Zeland IE3D, etc.

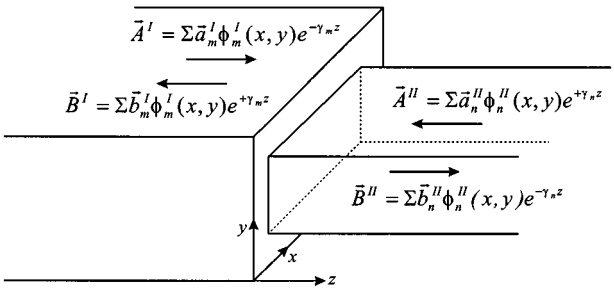

Fig. 1. Geometrical sketch and full-wave modal-expansion description of a rectangular waveguide step discontinuity.

SOC allows implementing a self-calibration procedure in the MoM scheme without resorting to any electrical parameters of uniform transmission line such as characteristic impedance and effective dielectric constant [12]–[15], as well as any presumed equivalent network topology of so-called port discontinuities caused by the impressed electric fields at the ports [7], [16].

The purpose of this paper is to examine the SOC scheme by revisiting a microstrip step discontinuity [17] that can reveal interesting properties of the SOC applications. This step structure itself is one of the most common microstrip lumped elements and its equivalent-circuit model was studied in the 1970s [18]–[22] based on static methods or experimental procedures. Since then, research has been oriented to full-wave simulations of its S-parameters [23], [24] using the MoM or other numerical methods. In this case, the obtained two-port S-parameters are basically dominated by the ratio of two strip widths rather than the step discontinuity itself. Thus far, no study has actually been carried out on the extraction of its equivalent dynamic circuit model from a full-wave MoM simulation. Our effort here is to show the origin of numerical errors existing in the three-dimensional (3-D) MoM and how they can effectively be calibrated through the SOC scheme that is validated by a number of comparisons. Two microstrip step discontinuities are formulated in terms of their equivalent dynamic circuit model over a wide frequency range.

II. Numerical Errors and SOC Technique

Let us begin with the description of physical mechanism of the numerical errors in the deterministic MoM modeling of a planar microstrip step discontinuity with reference to a modal-expansion characterization of waveguide step discontinuities [25]. Fig. 1 shows the geometry of a waveguide step discontinuity formed over the interface of two rectangular waveguides of different width and height. According to the modal-expansion approach, transverse electric or magnetic fields in the two waveguides ($\vec{A}^I$, $\vec{B}^I$, $\vec{A}^{II}$, and $\vec{B}^{II}$) can be formulated in terms of a superposition of transverse mode functions ($\phi_m^I(x, y)$, $\phi_m^I(x, y)$, $\phi_n^{II}(x, y)$, and $\phi_n^{II}(x, y)$) and longitudinal functions ($e^{-\gamma_m z}$, $e^{+\gamma_m z}$, $e^{+\gamma_n z}$, and $e^{-\gamma_n z}$, respectively), in relation with forward and backward directions, as depicted in Fig. 1. The continuity of transverse fields at the step plane ($z = 0$) yields unknown modal-expansion coefficients ($\vec{a}_m^I$, $\vec{b}_m^I$, $\vec{a}_n^{II}$, and $\vec{b}_n^{II}$). Due to the unambiguous definition of the wave impedance in a rectangular waveguide, the equivalent-circuit model can analytically be derived on the basis of an explicit relationship between the field theory-based S-parameters and circuit network-based Y- or Z-parameters.

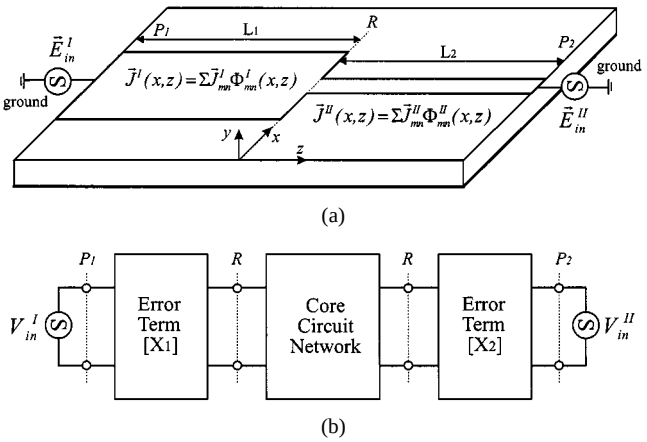

Fig. 2. Physical MoM layout and its equivalent network description of a generalized microstrip step discontinuity. (a) Admittance-type MoM scheme. (b) Equivalent network description.

Following this description, the incident and reflected fields in each waveguide can exactly be expressed in terms of modal expansion functions without the introduction of any impressed source fields at external port. However, an impressed source field, or sometimes called "excitation mechanism" [1]–[4], has to be assumed in the deterministic MoM characterization of the microstrip step discontinuity, as illustrated in Fig. 2(a), for the admittance-type MoM algorithm. Since this impressed field or voltage excitation approximately represents the realistic field distribution of quasi-TEM mode at ports of the two feeding lines, it brings about a numerical error at the source port called "port discontinuity," as discussed in [7] and [16], which is quite similar to the discontinuity of coaxial-to-microstrip transition in microwave measurements. This port discontinuity may approximately be modeled as a pure shunt capacitance [12] and more accurately considered as a shunt capacitance and series inductance [16] at low frequency. As frequency increases, the effects of such a discontinuity appear to be strongly frequency dispersive, as depicted in [16].

On the other hand, the longitudinally z-varied fields in rectangular waveguide are modeled in terms of the exponential functions, as in Fig. 1, which exactly describe propagation characteristics of multiple TE and/or TM modes in the uniform waveguides. In other words, no numerical discretization is required along the longitudinal z-direction due to the transverse modal expansion. With reference to Fig. 2(a) for the MoM, however, the overall conducting strip surface is discretized into a number of small cells along the x- and z-axis so that electric current densities over the strip surface ($\vec{J}^I(x, z)$, and $\vec{J}^{II}(x, z)$) can be calculated in terms of basis functions ($\Phi_{mn}^I(x, z)$ and $\Phi_{mn}^{II}(x, z)$, respectively). Strictly speaking, the mathematical expression of those current densities along the longitudinal z-direction is theoretically approximate as compared with a two-dimensional (2-D) MoM modeling of uniform microstrip line. Therefore, the inconsistency of 2-D and 3-D MoM characterization of microstrip feed line contributes to the other numerical error that should be frequency

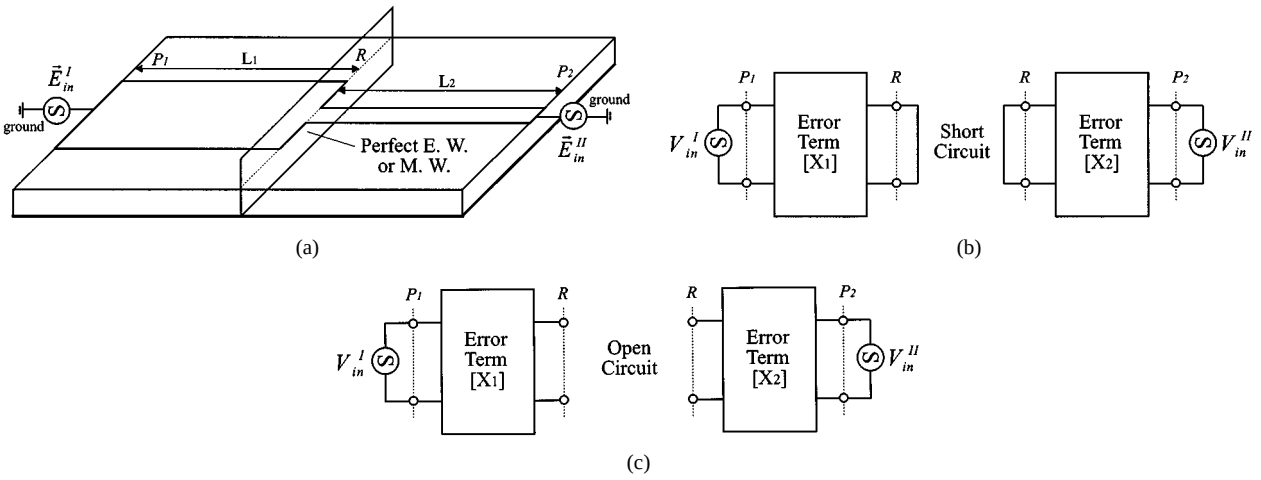

Fig. 3. Physical MoM formulation and equivalent network description of the two SOC calibration standards (*short* and *open elements*) with regards to the two external microstrip lines. (a) MoM formulation of the two SOC standards. (b) Network description of the two short elements. (c) Network description of the two open elements.

dispersive and also dependent on the truncated feed-line length or geometry in general. As discussed in [12]–[15], this error can be reflected in the difference between 2-D and 3-D MoM-based characteristic impedances and effective dielectric constants of a uniform microstrip line.

Thus far, the two inherent numerical errors in a deterministic 3-D MoM algorithm have physically been explained. To effectively make a calibration of those errors, they may be considered as a whole such that a single error term or box can be formulated for each feed line driven by the impressed voltage. Furthermore, the overall step discontinuity layout of Fig. 2(a) may be classified into the two distinct parts: core circuit network and two different error terms at the two sides, as depicted in Fig. 2(b). These two error terms exactly represent electrical behaviors of two microstrip lines between the source ports (P_1 and P_2) and the step interface (R), as in Fig. 2(a), respectively. The core network is the equivalent-circuit model to be deembedded or extracted from the full-wave MoM simulations.

In [11], the numerical SOC technique was originated and developed to accomplish this task by defining a pair of ideal calibration standards, namely, short and open elements, which are self-consistently developed in the 3-D MoM framework. Regarding the present step discontinuity, those elements of calibration can simultaneously be formulated for two feed lines by vertically inserting infinitely large electric and magnetic walls, respectively, at the step location (R), as illustrated in Fig. 3(a). The resulting perfect walls represent the ideal microstrip short and open ends in theory. In fact, they can simply be realized by applying an additional image counterpart [4] of the layered dyadic Green's functions with respect to the vertical plane at the step location (R). Fig. 3(b) and (c) is the equivalent-circuit description of two electric-field-excited feed-line sections separated by the electric or magnetic walls, as in Fig. 3(a). Without ambiguity, we can identify and isolate the two error terms (X_1) and (X_2) of Fig. 2(b) driven by impressed voltages and terminated by ideal short-/open-ends.

Considering the asymmetrical two-port topology of each feed line under the impressed fields in the 3-D MoM, the resulting error networks should have three independent parameters. As the electric current densities over the strip surface are numerically solved in the 3-D MoM, the three electric currents, namely, two port currents related to the short/open circuits, as well as the current flowing at the short-end, can easily be derived. Using the additional condition of reciprocity theorem, the obtained currents allow an explicit formulation of the error terms to be equivalent $ABCD$-matrix networks, as detailed in [11]. As the two different error terms in Fig. 2(b) are evaluated, the core circuit model can be deduced based on a simple cascaded transmission-line theorem. In the following, this SOC technique is deployed to extract the dynamic circuit model of the microstrip step discontinuity together with the conventional transmission-line deembedding technique, yielding a clear picture of the SOC scheme in a comparative manner.

III. Circuit Model and Numerical Convergence

Fig. 4(a) depicts the geometry of a microstrip step discontinuity, whose two feed lines present different strip widths (W_1 and W_2) and also transversely aligned by an offset distance (t) at the step location (R). Early work based on static assumption [18]–[22] suggested that the symmetrical counterpart with $t = 0$ in Fig. 4(a) could be expressed as a lossless equivalent T-type lumped-circuit network with a single shunt capacitance (C_g) and two series inductances (L_{p1} and L_{p2}), as illustrated in Fig. 4(b). As frequency increases, however, the static model has to be modified into a dynamic T-type circuit model that can account for all potential effects around the step discontinuity such as high-order modes, frequency dispersion, and radiation loss. Fig. 4(c) illustrates the complete circuit model with a shunt capacitive admittance ($Y_g = G_g + jB_g$) and two series inductive impedances ($Z_{p1} = R_{p1} + jX_{p1}$ and $Z_{p2} = R_{p2} + jX_{p2}$), which demonstrate electrical properties of this step discontinuity without any hypothesis in theory.

In the last two decades, almost all of the deterministic MoM algorithms have been developed under a common assumption in that the numerical error caused by the impressed field can automatically disappear as the source ports are chosen far away from the core discontinuity block. Nevertheless, no robust work

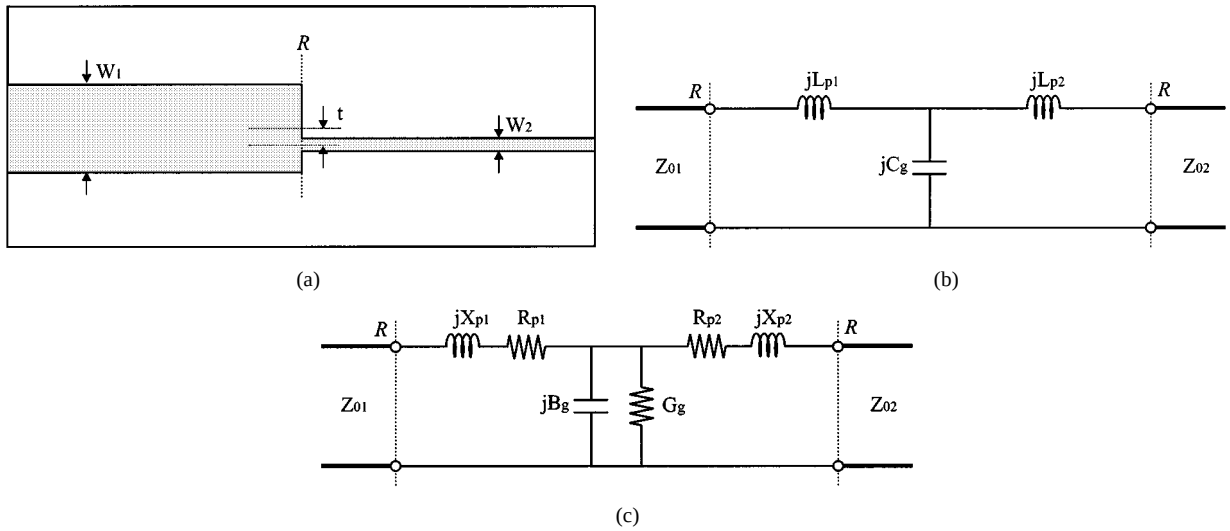

Fig. 4. Geometrical sketch and dynamic equivalent-circuit model of a generalized microstrip step discontinuity. (a) Geometrical sketch. (b) Static circuit model. (c) Dynamic circuit model.

thus far has been reported to prove that is the real case even though it is suggested that the port location should be chosen about quarter-wavelength away from the reference plane. As pointed out in [11], however, the deembedded circuit parameters are found very sensitive to the selected port locations along the feed line under this assumption. To our conceptual understanding, the above numerical errors including the port discontinuity cannot be negligibly small and they always involve themselves in the MoM-calculated parameters at each port. For the purpose of quantitative verification, the conventional transmission-line deembedding technique [1]–[4], called the Z_0-scheme, is simultaneously applied here to implement an alternative deembedding procedure based on the 2-D electrical parameters of a uniform line, i.e., characteristic impedance (Z_0) and effective dielectric constant (ε_{re}).

In the following, these two numerical deembedding techniques are used to deembed or extract dynamic parameters of the equivalent-circuit model, as illustrated in Fig. 4(c), from the MoM-simulated port currents and voltages at two ports, i.e., P_1 and P_2. To investigate the numerical instability due to the errors along the feed lines, geometry-dependent behavior of all the deembedded circuit parameters are studied with respect to different port locations from the step discontinuity. Fig. 5 depicts two groups of deembedded shunt or mutual susceptance (B_g) and self reactances (X_{p1} and X_{p2}) versus port-to-step distance ($L_1 = L_2$) at the frequency of $f = 6.0$ GHz. Looking at Fig. 5(a), the Z_0-based shunt parameter (B_g/ω) seems to be seriously varied as a function of the port location while the SOC-extracted B_g/ω consistently converges to the value, i.e., 0.043 pF, as L_1 and L_2 are extended beyond 3.2 mm. Similarly, we can find from Fig. 5(b) that the Z_0-based parameters (X_{p1} and X_{p2}) are unstably shifted up and down with respect to L_1 and L_2, while their SOC-based counterparts appear to achieve a rapid and stable convergence. These results exhibit well the noise-involved instability in the conventional Z_0-based technique and also demonstrate that the proposed SOC technique can effectively address such a problematic issue that is caused by the two aspects of the above-described numerical errors.

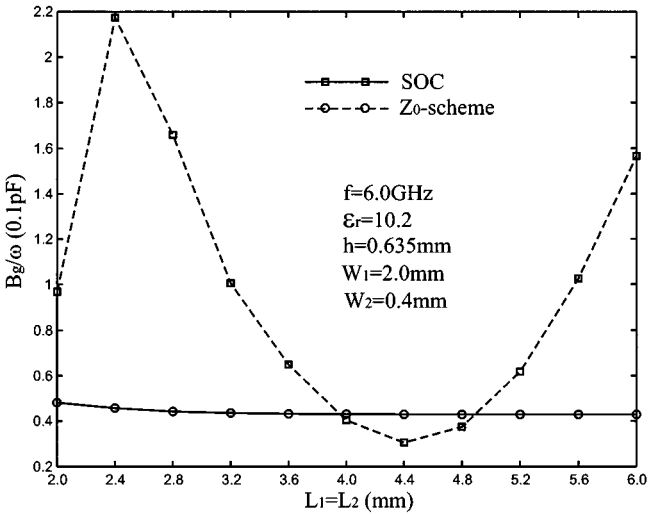

Fig. 5. Geometry-dependent characteristics: Extracted mutual-susceptance (B_g) and two self-reactances (X_{p1} and X_{p2}) versus the port-to-step distances ($L_1 = L_2$) along the two external microstrip lines using the Z_0-based and SOC deembedding procedures. (a) B_g. (b) X_{p1} and X_{p2}.

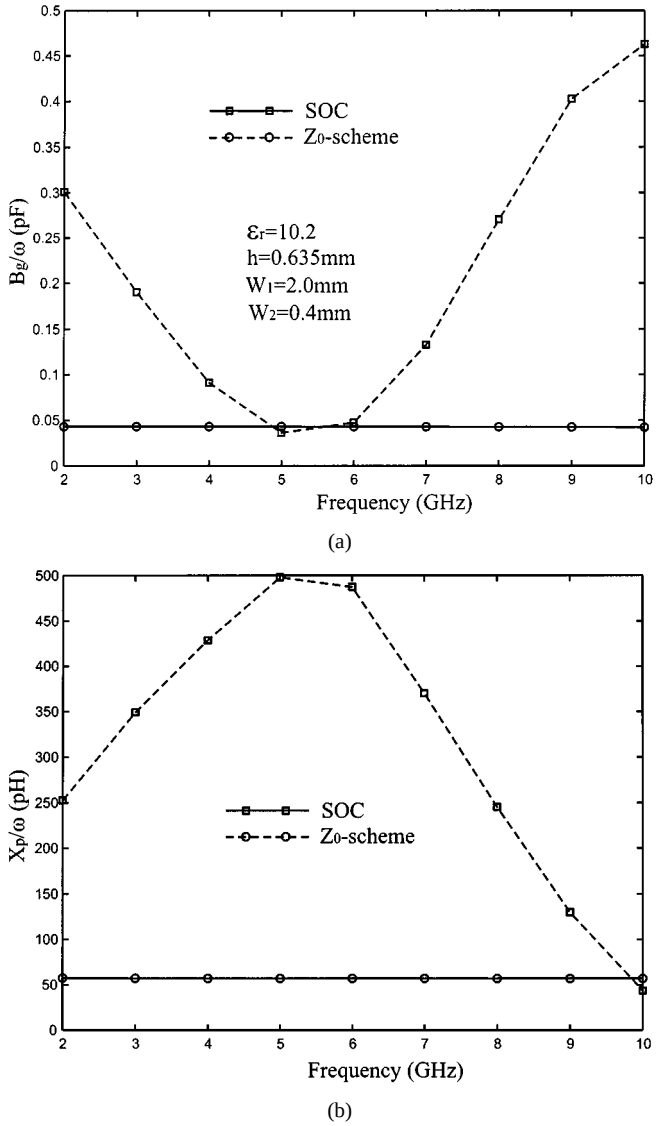

Fig. 6. Frequency-dependent characteristics: Extracted mutual-admittance ($Y_g = G_g + jB_g$) and total self-reactance ($X_p = X_{p1} + X_{p2}$) at a fixed port-to-step distance ($L_1 = L_2 = 5.2$ mm) using the two different deembedding procedures. (a) B_g. (b) X_p.

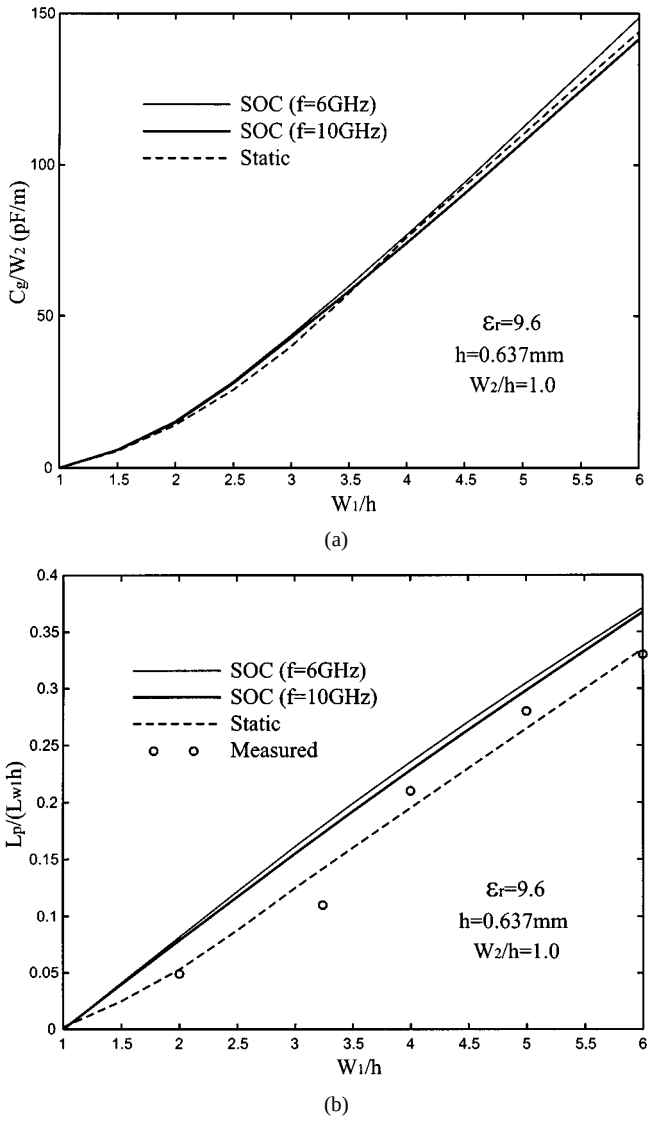

Fig. 7. Comparison of equivalent-circuit model parameters (C_g and L_p) versus strip width (W_1) at a fixed $W_2/h = 1.0$ among the SOC extracted, static, and measured results that were reported in [19] and [20].

IV. SOC-Extracted Circuit Model

In this section, the equivalent dynamic circuit models of both symmetrical and asymmetrical microstrip step discontinuity are studied over a wide frequency range through the validation of SOC-extracted parameters against the available static model parameters [18]–[22]. Prior to doing that, the SOC-extracted circuit model parameters are again illustrated versus frequency, as shown in Fig. 6, together with the Z_0-based ones for the same step discontinuity, as discussed above. We can see from Fig. 6(a) that the Z_0-based mutual B_g/ω moves up and down over the frequency range (2.0–10.0 GHz), thereby showing a frequency-dependent numerical instability. In the meantime, the SOC-extracted mutual B_g/ω remains almost unchanged, which represents a shunt capacitance in a static model in Fig. 4(b) [18]. Otherwise, Fig. 6(b) indicates that the Z_0-based X_p/ω ($=X_{p1}/\omega + X_{p2}/\omega$) appears irregularly varied against frequency. However, the SOC-extracted X_p/ω remains a frequency-independent constant (approximately 57.0 pH), thus representing the equivalent series inductances in a static model in Fig. 4(b) [18]. The results in Fig. 6 show us that our SOC can also avoid the frequency-related numerical instability that is observed in the conventional technique.

As mentioned before, no field theory-based extraction of this step discontinuity has been reported thus far and also all the S-parameters based on the experimental deembedding techniques are not suitable for the extraction of Y- or Z-matrix circuit model of planar circuits. Thus, this is the only way for us to validate the accuracy of our SOC-extracted circuit model through comparisons with the published static circuit models derived from quasi-TEM analysis and indirectly resonance-type measurement procedure [18]–[22]. Fig. 7 shows the shunt capacitance (C_g) and series inductance (L_p) per unit length of a wide strip width (W_1) versus W_2/h of a narrow strip at two different frequencies. It can be seen from Fig. 7(a) that the SOC-extracted C_g is in excellent agreement with its static counterpart from [20]. SOC-extracted L_p also agrees well with static and measured results in [19], as illustrated in Fig. 7(b).

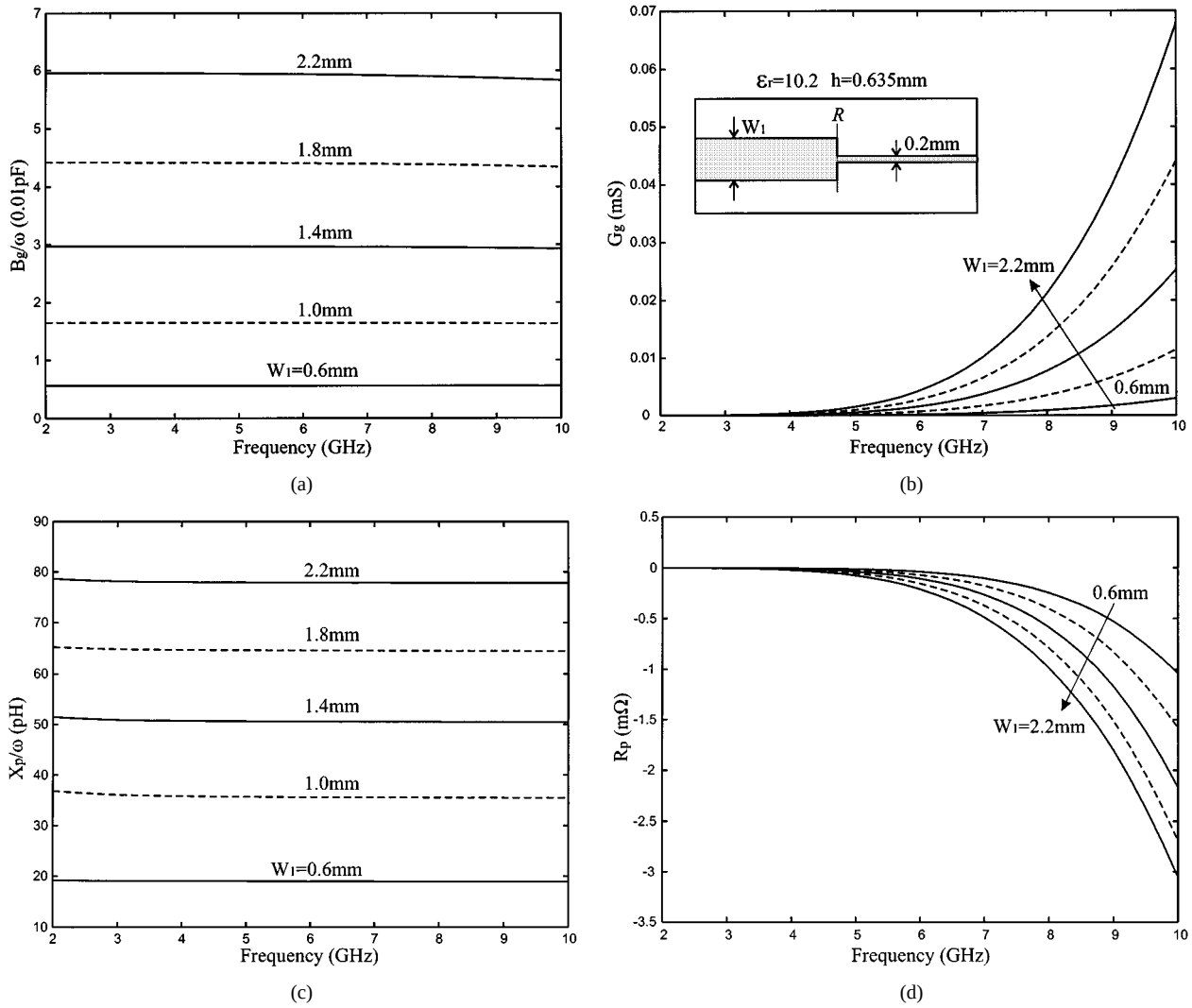

Fig. 8. Frequency-dependent SOC-extracted circuit model parameters for a symmetrical microstrip step discontinuity with different width W_1 at a fixed $W_2 = 0.2$ mm. (a) B_g. (b) G_g. (c) X_p. (d) R_p.

Therefore, the equivalent-circuit models of two types of microstrip step discontinuities are obtained to demonstrate their complete dynamic electrical properties for the symmetrical structure as a function of ratio (W_1/W_2) and for the asymmetrical structure as a function of offset distance (t), respectively. Fig. 8 depicts the SOC-extracted parameters versus frequency under a different strip width (W_1) and a fixed strip width ($W_2 = 0.2$ mm) for the symmetrical case. In Fig. 8(a), the parameter (B_g/ω) is found almost unchanged with frequency for different strip width (W_1), thus exhibiting a lumped shunt capacitance [17], while its value rapidly goes up as W_1 is widened. In Fig. 8(b), SOC-extracted shunt conductance (G_g) seems to change exponentially with frequency and quickly goes up with W_1. This represents a radiation behavior of the equivalent slot aperture with the length (W_1–W_2) at the step location (R).

SOC-extracted series inductive parameter (X_p/ω) is plotted in Fig. 8(c), which also remains unchanged with frequency, indicating a lumped series inductance. Furthermore, this equivalent inductance is largely enhanced as W_1 becomes widened, due to the increasing curvature extent of the current density flowing from longitudinal to transverse orientation on the wide strip conductor around the step interface. The series resistance (R_p) is found very small in the symmetrical case and its results are plotted in Fig. 8(d). As W_1 increases to 2.2 mm, R_p achieves its maximum absolute value, i.e., 0.0031 Ω at $f = 10.0$ GHz. This extremely small negative value may represent the EM power exchange between the series and shunt parameters in this T-type network and can be ignored in the circuit model in Fig. 4(c).

Fig. 9 depicts SOC-extracted model parameters for the asymmetrical step discontinuity having different offset distance (t). As shown in Fig. 9(a), the shunt (B_g/ω) still shows a good frequency-independent capacitance behavior within the maximum range of 2.0% over the frequency bandwidth of 2.0–10.0 GHz. Otherwise, its value is slightly raised from approximately 5.8 to 7.0 pF, as the offset t increases from 0 to 1.0 mm. In parallel, the shunt G_g remains almost unchanged even though t is enlarged to 1.0 mm. The result in Fig. 9(b) indicates that the radiation-related shunt conductance (G_g) is hardly affected by the offset and mainly determined by the equivalent aperture length (W_1–W_2) in the asymmetrical case. However, it is not always true for the equivalent series admittance parameters. In Fig. 9(c),

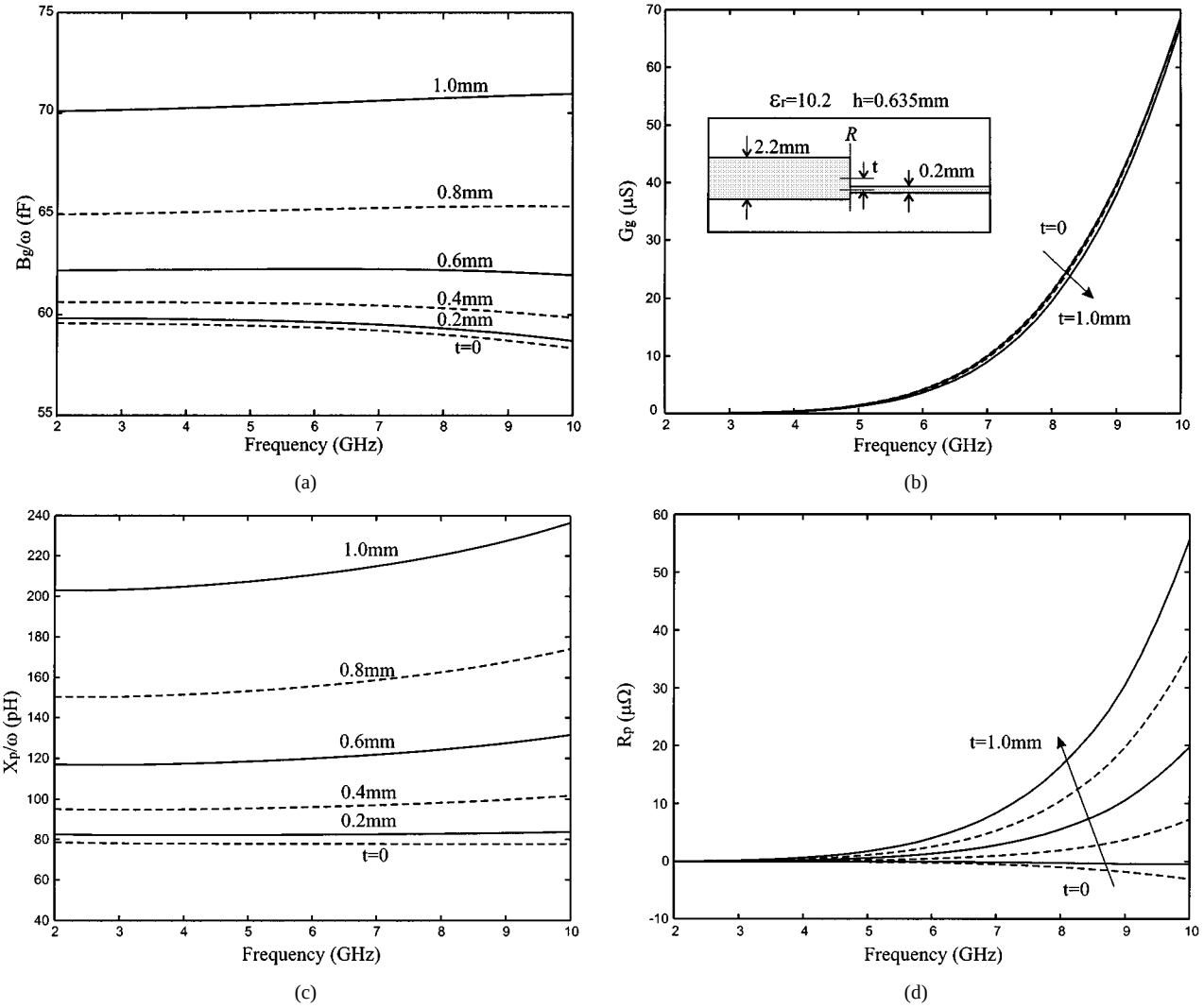

Fig. 9. Frequency-dependent SOC-extracted circuit model parameters for an asymmetrical microstrip step discontinuity with different offset distance (t). (a) B_g. (b) G_g. (c) X_p. (d) R_p.

we can see that the parameter (B_p/ω) still goes up rapidly as W_1 is widened, but it gradually manifests a nonlinear frequency-dependent variation as offset t increases. Strictly speaking, the series B_g should be perceived as a frequency-dispersive inductive reactance instead of a lumped series inductance in the symmetrical case. On the other hand, the series resistance (R_p) is found from Fig. 9(d) to gain a significant enhancement as offset t increases to a great extent and also vary exponentially with frequency. This phenomenon is mainly attributed by the fact that different transverse [upward and downward in Fig. 9(b)] orientations of the two current densities flowing on the wide strip conductor around the step interface lead to an enhancement of radiation power as t increases. Accordingly, the relevant lossy series resistance should be taken into account in the complete dynamic circuit model, as in Fig. 4(c), for the asymmetrical step discontinuity.

V. Conclusions

In this study, the SOC technique has been developed in the deterministic MoM algorithm for field theory-based deembedding and extraction of planar integrated circuits or discontinuities. With reference to the modal-expansion characterization of waveguide step discontinuity, two aspects of numerical errors, namely, port discontinuity and inconsistency of the 2-D and 3-D MoM, have been physically explained through the modeling of microstrip step discontinuity. Equivalent-circuit models have been derived from both SOC and conventional techniques, which allow systematic comparisons between the two schemes. Results have shown harmful effects of these numerical errors in deembedded parameters, in particular, geometry- and frequency-dependent numerical instability found in the conventional technique. Furthermore, it has been shown that such numerical noises can completely be calibrated in our SOC scheme. SOC-extracted circuit model parameters have been validated by those obtained from previous static analysis and experiments.

Without any pre-assumption in theory, our results have shown, for the first time, equivalent dynamic circuit models for both the symmetrical and asymmetrical microstrip step discontinuities. It has been found that the symmetrical case can simply be perceived as a shunt capacitance and a conductance, as well as two series small inductances. However, the

asymmetrical case has a different lumped model behavior, and it should be modified as two series inductive reactances and resistances in addition to the shunt capacitance and conductance. The proposed SOC technique is believed to have an unparalleled capacity in parameter extraction of planar circuits, which certainly allows bridging the huge gap between the field theory-based modeling/simulation and circuit network-based synthesis/optimization. Moreover, the proposed numerical calibration concept should also be applicable to other modeling techniques.

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